

Trade-off Study on Switched Capacitor Regulators for Implantable Medical Devices

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Abstract—This study presents the trade-offs when using a Switched capacitor (SC) DC-DC converter as the energy management device on a highly integrated implantable medical device. The efficiency of the *Low Dropout Regulator (LDO)* is presented and used as a reference point to determine the performance gain when using an SC converter. Also, the balance between load requirements and optimum parameters for implementing an SC converter is analyzed. The analysis presented can be used to determine when an SC converter is the best solution for energy management on an implantable device.

Index Terms—Switched capacitor circuits, DC-DC power converters, Switching converters, Microelectronic implants

I. INTRODUCTION

IMPLANTABLE medical devices have as main requirements the use of highly integrated components and to use very low energy levels. CMOS technologies have made it possible to reduce the quantity, size and power of the circuitry required to perform signal sensing and processing, data storage and transmission/reception of information. Fig. 1 shows that besides the mentioned functions, the implantable device also requires elements for energy reception, storage and management.

The energy can be supplied by means of a power harvesting technique (e.g. magnetic link) or it could be stored in an element present on the same implant (e.g. a battery), also some implants rely on both energy sources. Due to limited size for components and also the environment where the implant has to be placed, either energy supply source can only provide small amounts of energy to run the implant. This constraint is addressed by optimizing the power consumption of every element on the implant. In the case of the power management unit, it should be as efficient as possible in terms of low power loss and reduced quiescent current.

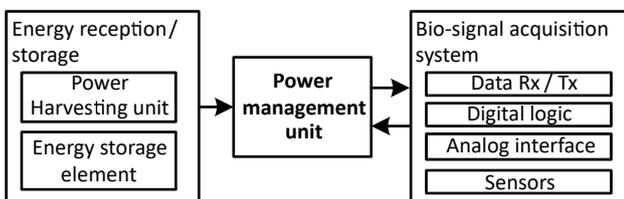


Fig. 1. High level view of a basic implantable device structure.

A common element used for controlling the power provided to the electronics on integrated circuits is the *Low Dropout*

Voltage (LDO) regulator, as in [1]. However, the use of an LDO might not be the best fit for a low power implantable device. *Switched capacitor (SC) DC-DC converters* represent an alternative to LDOs on low power implantable devices.

II. LDO EFFICIENCY ANALYSIS

Fig. 2 presents the basic structure of an LDO regulator. The output voltage V_o is regulated by controlling the source-drain resistance of the PMOS transistor. This resistance is controlled by the output of an operational amplifier forming a negative feedback loop. In the case of the LDO, there is a first source of loss due to the current flowing through the operational amplifier, the resistive voltage divider and the voltage reference generator; the sum of these currents is called quiescent current I_q (in the case of Fig. 2, $I_q = I_{amp} + I_{rfb}$). The quiescent current can be reduced by optimizing the LDO components making it negligible when compared to the load current consumption. However, the main cause of loss is the power dissipated on the PMOS source-to-drain resistance.

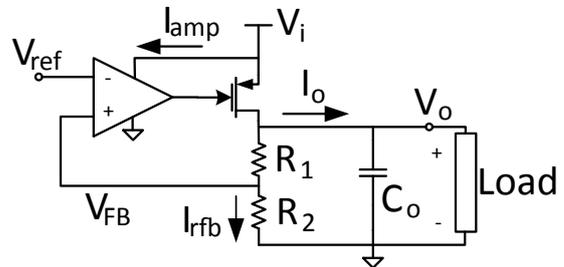


Fig. 2. Basic architecture of an LDO.

Given that the efficiency of a regulator is the ratio of output power over the input power, then the efficiency for an LDO is given by:

$$\eta = \frac{P_{in}}{P_{out}} * 100 = \frac{I_o V_o}{(I_o + I_q) V_i} * 100; \quad (1)$$

This equation shows how the maximum efficiency on an LDO regulator is highly dependent on the difference between input and output voltage. The difference between these two voltages is proportional to the power that is dissipated, as heat, in the PMOS resistance. The LDO efficiency increases as the difference between input and output voltage decreases.

From this analysis it is possible to conclude that an LDO is not suitable for applications where the input voltage can have a large difference with the output voltage. In the case of implantable devices, the difference between the input voltage and the core voltage of the electronics in the implant can be large.

III. SWITCHED CAPACITOR REGULATOR POWER LOSS ANALYSIS

The SC-converters are a sub-set of the switched DC-DC converters. This kind of switched converter is ideal for implementations on standard CMOS technology given the fact that it only requires switches and capacitors which can be easily integrated. Some other kinds of switched regulators make use of inductors, making them less appealing for a highly integrated application even when these offer a better efficiency.

A general model [2] for a SC-converter is presented in Fig. 3. As shown, the SC-converter is modelled as an ideal transformer with a voltage gain of n/m . The power at both sides of the ideal transformer are the same so no energy loss is present. When no load is present, the SC-converter provides the nominal voltage gain. When the load is present, the output R_o resistance models the power loss due to the charge and discharge of capacitors (re-distribution loss), the presence of this equivalent resistance produces a drop in the output voltage at the load. Following, the analysis of the power loss of the SC-converter and a more detailed model are presented.

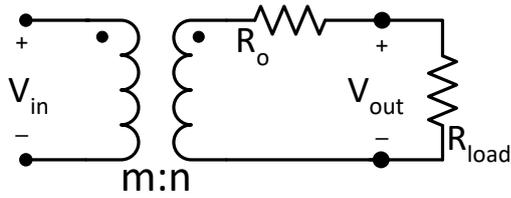


Fig. 3. Basic model of an SC-converter.

These converters are based on the transfer of charge from the input to the output by using capacitors that are switched between two phases: charge and discharge. In the first phase the capacitors are charged to a given voltage from the input. Then in the second phase, the accumulated charge is transferred to the output node. An example of an SC-converter is presented in Fig. 4.

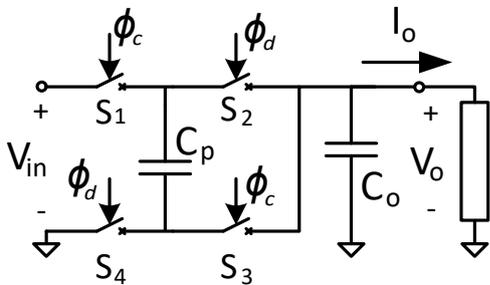


Fig. 4. Two phase switched capacitor DC-DC converter with ideal conversion ratio 2:1.

The converter presented in the image has a nominal conversion gain of $1/2$, which means that ideally the output voltage is equal to half the input voltage. During the charging phase ϕ_c , the switches S_1 and S_3 are closed so the pumping capacitor C_p is charged to $V_{in} - V_o$. Then in the discharging phase ϕ_d , the capacitor is connected in parallel to the output through the switches S_2 and S_4 . In this phase the capacitor discharges to V_o . Assuming that the switching frequency is $F_s = 1/(T_c + T_d)$, equal charging and discharging times and that the equivalent resistance on every path (charge/discharge) is R_{sw} . Based on the previous and the analysis in [3], [4] and [5], the output voltage is given by:

$$V_o = \frac{1}{2}V_i - \frac{I_o}{8C_p F_s} \coth\left(\frac{1}{4R_{sw}C_p F_s}\right) \quad (2)$$

where C_p , F_s and R_{sw} are the pumping capacitors capacitance value, the switching frequency and the *on-resistance* of the CMOS switches, respectively.

From this expression it can be noted that there is a deviation between the nominal gain ($1/2$) and the effective gain of the converter.

This first loss is due to the limited pumping capacitor size and sampling frequency. The power that is lost is dissipated in the form of heat when the current I_o goes through the *on-resistance* of the switches present on the charge/discharge paths. The *on-resistance* of the CMOS switches is given by:

$$R_{sw} = \frac{1}{\mu_{eff} C_{ox} (W/L) (|V_{gs} - V_{th}|)} \quad (3)$$

By using the model presented in Fig. 3 and (2), the output resistance of the converter R_o , which is causing the voltage drop from the ideal $V_o = V_i/2$, is given by:

$$R_o = \frac{1}{8C_p F_s} \coth\left(\frac{1}{4R_{sw}C_p F_s}\right) \quad (4)$$

Based on (3) and (4) it is possible to establish that the power loss can be reduced by setting appropriate values for the pumping capacitors, the switching frequency and the CMOS switches dimensions (to reduce R_{on}).

The loss factor present in (2) is not the only one affecting the performance of a SC-converter. Besides of the effect of the *on-resistance* (R_{on}) of the non-ideal CMOS switches, the gate of every switch has a gate capacitance that has to be charged and discharged on every phase of the switching clock, which translates to the power loss given by:

$$P_{sw} = (F_s C_{ox} W L V_{gs}) V_{gs} \quad (5)$$

Also in a CMOS device, the pumping capacitors present a parasitic capacitance from the bottom plate to the substrate. Depending on the architecture of the switched regulator, this capacitance is charged and discharged during the switching cycle. In the case of the 2:1 SC-converter, the power loss due to this parasitic capacitance is:

$$P_{par} = (A_{cp} C_{bp_s} F_s V_o) V_o \quad (6)$$

where A_{cp} is the pumping capacitor area and C_{bps} is the capacitance per area from the bottom plate of the capacitor to the substrate.

Using the results from (4), (5) and (6), it is possible to model the SC-converter as shown in Fig. 5

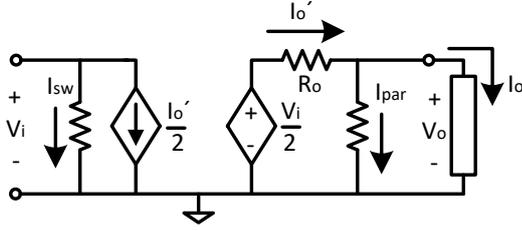


Fig. 5. Detailed model for the SC-converter with conversion ratio 2:1.

On this model the current I_{sw} is the equivalent current due to the switching loss P_{sw0} , which is computed as the sum of the loss on every switch on the SC network. In the same way, the current I_{par} is the equivalent current of the power loss due to the parasitic bottom plate capacitances.

IV. TRADE-OFFS FOR SWITCHED CAPACITOR REGULATORS

The model presented in the previous section makes computing the efficiency of the SC-converter possible. Fig. 6 presents the efficiency, of a 2:1 SC-converter, versus the input and output voltage ratio

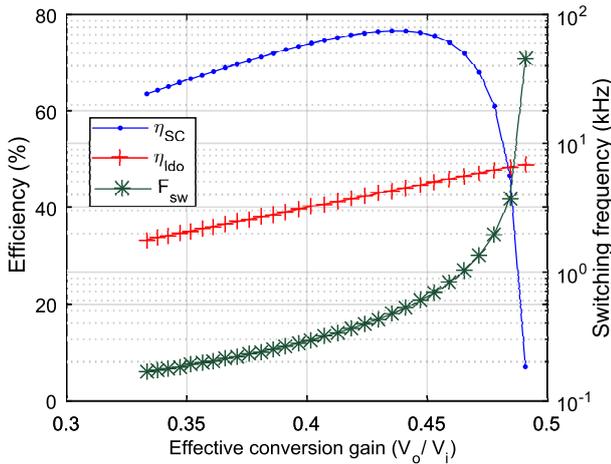


Fig. 6. Efficiency comparison between an SC-converter and an ideal LDO. Also the switching frequency for the SC-converter is shown. The load current is $100nA$ (The simulation used the AMS350 CMOS technology parameters).

As shown in the figure, the efficiency of the SC-converter presents a limited range of conversion gain, due to the two components of power loss. At low frequencies the conduction loss is prevalent, while at higher frequencies the dynamic loss reduces the performance. However, it is important to note that for most of the operational range of the SC-converter, its efficiency is larger than the LDO efficiency.

Theoretically the efficiency can be maximized for a given requirements set (V_o, I_o) by setting appropriate values for the switching frequency and the size of pumping capacitors

and switches. However, for certain application requirements, the required SC-converter settings can be restrictive due to area consumption (capacitors/switches too big) or because the cost of generating a high frequency switching clock would represent a high loss in efficiency (the previous analysis does not account for the power used for clock and voltage reference generation).

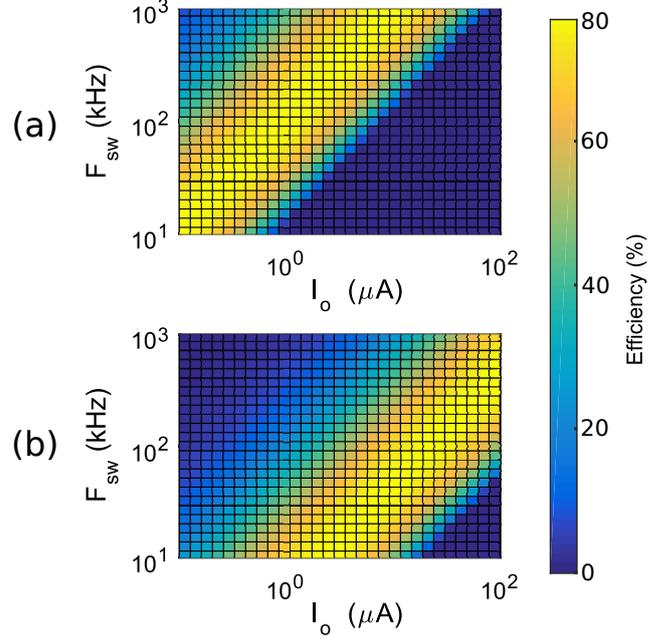


Fig. 7. Performance curves for the SC-converter for two set of sizing parameters (Switch Size, Pumping capacitor) for (a) Optimized for $100nA$, (b) Optimized for $100μA$ (The simulation used the AMS350 CMOS technology parameters).

Furthermore, when the load needs a quite large range of output current values, finding the optimal values can be difficult. As an example, Fig. 7 shows the efficiency computed for an SC-converter optimized for two different output current values ($100nA$ and $100μA$) which are the limits for the current range of a given load.

The figure shows how the performance for low load currents is reduced (for the same frequency) when using the optimal parameters for high load currents. Also, it is possible to notice a similar behavior when using the low current optimization and a large current is present at the load.

The designer has to optimize the system based on the average current expected at the output. Also, a large (calculated on the base of the maximum current and peak duration) external capacitance needs to be used to prevent a reduction on the output voltage when large currents are present.

The inherently limited conversion gain range and efficiency reduction at the limits of the SC-converter can be dealt with by using a reconfigurable SC-converter with multiple gains such as [6] and [7]. Fig. 8 presents the efficiency curve of a reconfigurable SC-converter with three nominal gains. As it can be noted from the curve, the use of these three nominal gains extends the effective conversion gain range of the system

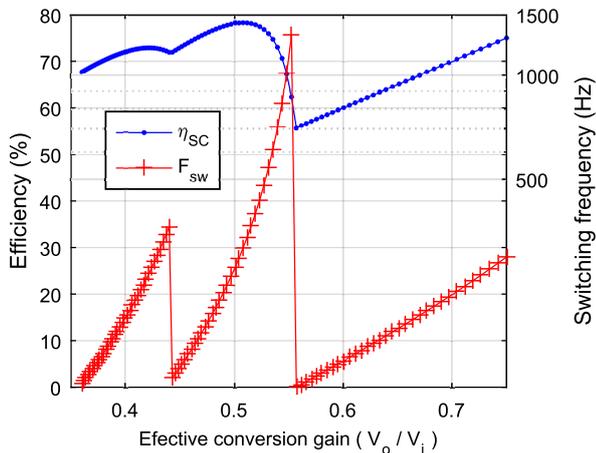


Fig. 8. Efficiency of a multi-gain SC-converter. The model simulated has three configurable gains: 1/2, 2/3 and 1 (The simulation used the AMS350 CMOS technology parameters).

when compared to the single stage system (Fig. 6), and also keeps a larger efficiency than the one present on a LDO. Each gain configuration is limited to a range where it can offer the maximum efficiency.

The SC-converter used to generate the curves in Fig. 8 uses two pumping capacitors in two clock phases. By adding extra pumping capacitors (and switches) to the system, more conversion gains can be configured. Enlarging the set of configurations on a re-configurable SC-converter has as result larger average efficiency values, however, the complexity of the system and the optimization of it also grows. Nevertheless, a highly re-configurable SC-converter is most effective especially for medical implants that use power harvesting elements as energy source. As an example, if the energy is provided by means of *wireless power harvesting*, the voltage that has to be regulated by the SC-converter can vary in a quite large range due to different alignments between the implant and the external transmitter, how deep the implant is inside the body (the distance between power transmitter and receiver) or fabrication mismatches on the harvesting elements, among others. Given this variation in the harvested voltage, it is important to have the largest possible conversion efficiency for its whole range.

V. CONCLUSION

This paper presents how the use of an SC-converter as the energy management element for implantable devices leads to power savings from the limited energy present in the implant. A mathematical model shows the variables that play a role in the efficiency of a single stage SC-converter. Furthermore, the interdependence between the optimal parameters and the system requirements, such as input voltage variation range and output current, is discussed.

In the specific case of using an energy harvesting unit as power source, the performance can be boosted by using a multi-gain SC-converter architecture. In this case the designer

must balance the performance requirements and the complexity of the system.

In the case of configurable SC-converters, the use of detailed mathematical models such as the ones presented on this document, makes it possible to obtain the optimal parameters for the design by using the input voltage range and the output voltage and current values as requirements. Also the optimum parameters are a function of the switching frequency, which has to be selected properly since the power (not accounted for this analysis) required to produce this signal is proportional to its frequency, therefore keeping the frequency as low as possible is needed for increasing the overall efficiency of the converter. However low frequency values lead to large capacitance values that will require large area in the integrated circuit. The designer has to use the results to find a balance between area and power requirements.

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